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Design of High Performance Double Tail Comparator Using Header Switch

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Abstract: Power consumption is most important parameter for concern in CMOS technology. For past several years, technology scaling is the most important procedure for the improvement of the performance of circuit in terms of the power, speed etc. In this paper, design and analysis of double tail comparator with sleep transistor is done in terms of power, delay and noise. Comparator is the very important circuit in the digital design and the performance of comparator is defined in terms of power and speed, which is the most important factor in attaining the complete performance of ADCs. Several ADCs require small delay, Low power comparators with small die size. It is observed that in the proposed comparator power, delay and pdp is reduced having values of $169.9e^{-9}$ watts, 319.7ps and $54.25e^{-16}$ respectively.

Key Words: ADC, Double-tail Comparator, Dynamic Comparator, Low power design.

I. INTRODUCTION

In the era of miniaturization, predictable CMOS Technology poses boundaries in Device physics scaling and interconnect, so the technology movement from micro to nano Electronics is the requirement of the present scenario, where all electronic equipment's or gadgets occupy the use of chips or die of one kind or the other and the key point lies in the process of cutting the chips down very small sizes keeping in mind the limit of area.

Our subject of interest is VLSI (Very Large Scale Integration), where thousands of transistors are implemented on a single chip and moreover the physical scaling of these CMOS transistors is accomplished in Nano scale regime. Recently, low-power and high-performance nano scale IC design is draw much attention due to the emerging needs for handy multimedia equipment's and the high-end processors. So reducing power consumption, propagation delay in VLSI's are the important design issues. More over in nano technology node different Performance criteria are also require interest to optimize the overall performance of design [1].

The Comparator design is an extremely essential and functional arithmetic constituent of digital arrangements. There are many approaching areas which is used to implementing CMOS comparators. The fundamental comparator circuit is used for comparison of the two different signals. One is the analog signal and other is the reference signal and the outcome of the comparison is in the form of binary signal.

From Fig.1 one can understand the operation of the comparator. V_{IN+} is the signal which is applied on the non-inverting terminal of the op-amp and V_{IN-} the signal which is applied on the inverting terminal of the op amp.

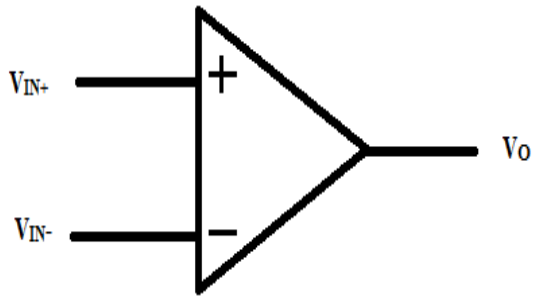

Fig.1.Comparator operation

If V_{IN+} is greater than the reference signal than the output is logic 1 and V_{IN-} is greater than the reference signal than the output is logic 0. So the output of the comparator gives decision according to the input provided at which terminal and whose value is greater than reference value [1].

$$V_{IN+} < V_{IN-} \quad \text{then } V_O = V_{SS} = \text{logic 0.} \qquad (1)$$
$$V_{IN+} > V_{IN-} \quad \text{then } V_O = V_{DD} = \text{logic 1.} \qquad (2)$$

Basically analog signal is the signal whose value is continuous in both time axis and amplitude axis. But Binary signal have only two values according to the input signal amplitude with respect to time. Because of these two values binary signal have two transition states. The outcome of comparator is in binary form so comparator also works in two transition states and changes their states in between two transitions. Because of these characteristics comparator is the most important circuit which is used in the process of converting analog signal into digital signal. So this circuit finds wide role in A/D conversion. In analog to digital conversion we first sample the input signal which is in analogous form with respect to time then quantize its value and encode it. Superscalar

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microprocessors make broad utilize of associative matching logic and comparators to maintain out-of-order implementation and virtual memory mechanisms [2].
In modern world of handy and portable devices like computers, mobile phone, laptops in which power is the major issue in VLSI designs. Power consumption is the topic of great interest. As we know that the batteries provide the limited power to the main device so the circuitry of the main device in such a way that it consume less power. Large power dissipation of the device require additional circuit which is costly used for noise compensation.

Comparators is the most important component in digital design so reducing the consumption of power in comparator circuit is one of the most important issue of low power design. There are many power saving procedures which is involved in the optimization of the sub threshold leakage current due to power supply results the variations in the circuits [3].

Factors like high speed, full swing output, and consumption of small power and high value of input impedance, regenerative dynamic latched comparator are widely important circuits for several applications like ADCs, data receivers, zero crossing detector and memory sensing applications [4]. The threshold voltage v_{th} is resulting because of the input reference voltage. Basically it is the latched offset voltage which resulting the current factor and mismatch between the parasitic capacitance and output load capacitance.

These capacitances limit the performance of comparator circuit. The input offset voltage can be obtained by using the pre amplifier stage of the latched circuit, but there is a disadvantage that the comparator having pre amplifier stage is undergo with the consumption of large power having larger bandwidth and because of reduction in the source to drain resistance, the gain of the circuit is also reduced [5]. Continuous technology scaling is cause of this reduction.

For past several years, technology scaling is the most important procedure for the improvement of the performance of circuit in terms of the power; speed etc. because of these scaling's, supply voltage and threshold voltage is reduced for the MOS transistors in submicron processes.
When the reduction in supply voltage occurs, the dynamic power is reduced but static power dissipation is increased due to the leakage current. Transistor dimensions are also a very important parameter to get the optimized performance of the circuit [6-7].

II. DYNAMIC COMPARATORS

Basic dynamic comparator has full output swing voltage and having larger input resistance and small leakage power consumption. The schematic diagram of the basic dynamic comparator is shown in Fig 2 [8]. In the operation of basic conventional dynamic comparator, there are two important phases. One is reset phase and other is decision making phase. In the time of reset phase the clock applied to the circuit is zero and tail transistors of the circuit is shut down or in off mode, and both the outputs which is out_n and out_p achieves a certain level V_{DD} because of transistor M_1 and M_4. In the decision making phase, we apply the clock signal which is equal to the supply voltage to the tail transistor and transistor become on.

Now when the input voltages is applied to the input terminals of the circuit, the out_n and out_p which is already pre charged with the V_{DD} is going to discharge with different discharging rate. If $V_{IN1} > V_{IN2}$, so Out_p will discharged sooner than Out_n which means Out_p to drop down to $(V_{DD}–V_{th})$ where V_{th} is the output voltage of the threshold voltage of the transistor where input V_{IN1} is applied.

When PMOS transistor will turn on, the latch restoration acquires by back-to-back inverters. Then, out_n started to charge to V_{DD} while out_p discharge to ground. The circuits perform their operation in reverse mode when V_{IN1} is less than V_{IN2} [9].

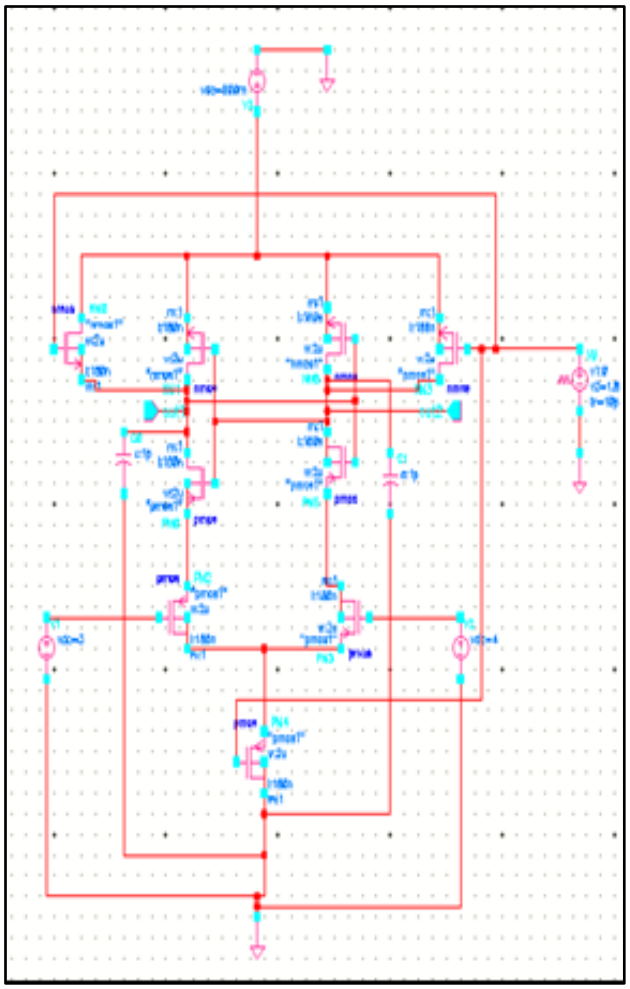

Fig 2. Schematic of Basic Dynamic Comparator

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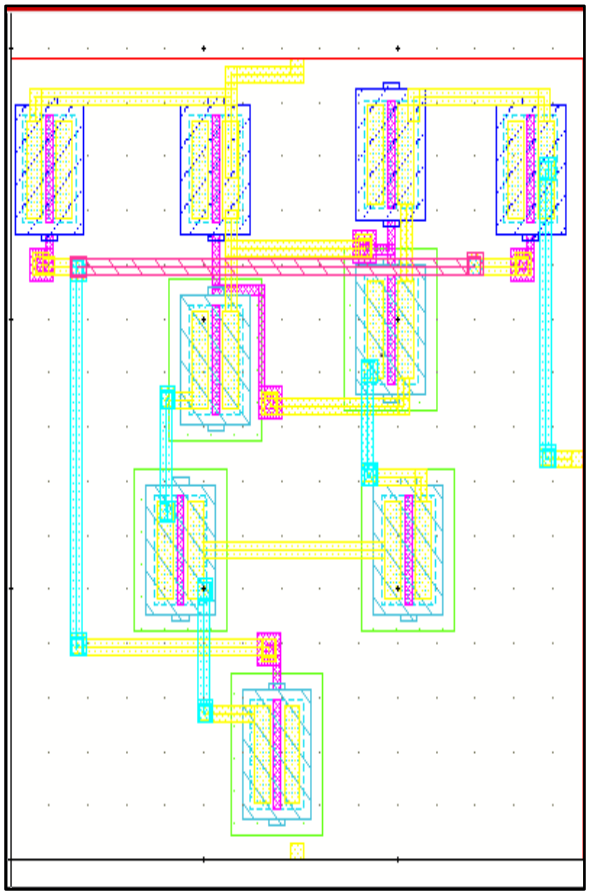

Fig 3. Layout of Basic Dynamic Comparator

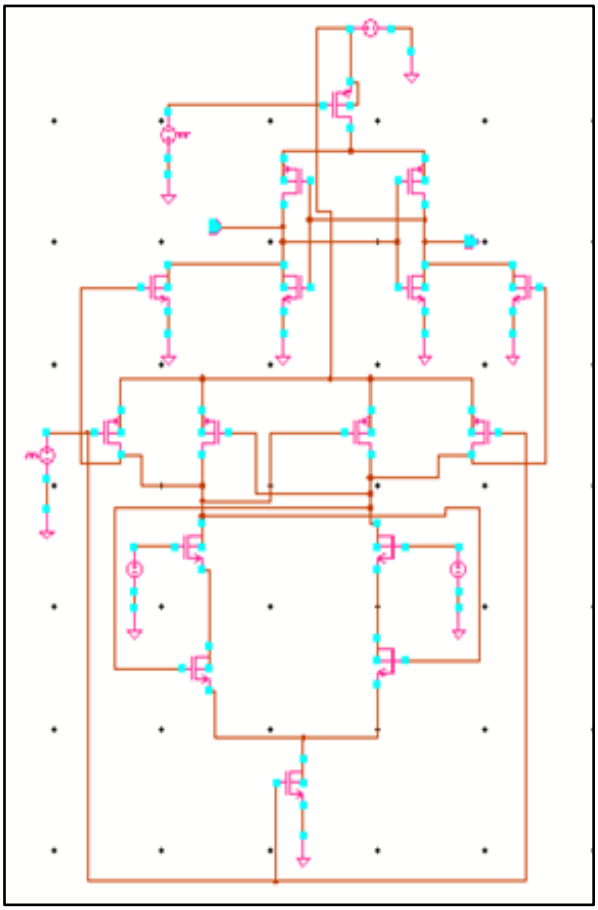

Fig 4. Schematic of Double Tail Comparator

In fig. 3, a conventional dual tail comparator is presented. In double tail comparator circuit have two transistors (PMOS and NMOS) in which clock is applied. This comparator can perform their function in small supply voltage as compared to conventional comparator.

This comparator provides large current to the latch and M_{tail2}, which provides the fast latched operation which do not depend upon input common mode voltage and to gain low offset it provide small current and M_{tail1}.

For their operation, comparator have two stages and is reset phase and second is decision making phase.in reset mode, clock is equal to zero, M_{tail1} and M_{tail2} is off. This condition allows turning on M_3 and M_4 transistor which pre-charge the f_n and f_p node to V_{DD}.

Because of this voltage transistors M_{RI} and M_{R2} is pull down the output voltage to the ground. In decision making phase, clock becomes V_{DD} and transistors M_{tail1} and M_{tail2} becomes ON. This condition causes to turn off M_3 and M_4. The voltage at nofe f_n anf f_p start to discharge with a rate if $I_{Mtail}/Cfn(p)$.

The transistor M_{R1} and M_{R2} passes the differential voltage to the back to back inverter and delivers a worthy protecting among input and output, causing in decreased rate of kickback noise [10].

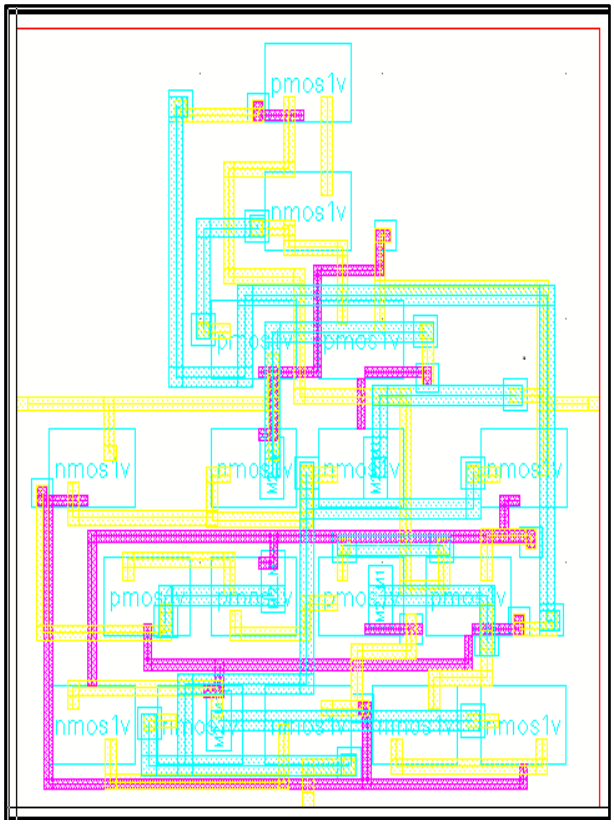

Fig 5. Layout of Double Tail Comparator

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III. DOUBLE TAIL COMPARATOR USING SLEEP TRANSISITOR

When we implement any circuit into hardware, power is the major issue for consideration. Total power is the combination of both static and dynamic power and 50% supply of total power dissipation is provided by dynamic power. So if we improve the technology scaling, the power consumption is decreased [11].

There are several procedures to decrease the consumption of power. Power gating is one of the techniques which is used to decrease thee static power consumption. This technique reduces the power when transistor is in idle state. A sleep transistor might be a NMOS or PMOS having larger threshold voltage V_{th}.

In this technique the concept of virtual supply V_{DD} and virtual ground is used. In these techniques sleep transistors are used. A sleep transistor can be put in the series with the circuit of low threshold voltage. The operation of this technique is performed in two different modes. One is active mode and second is sleep mode. In the operation of active mode, sleep transistors become on to perform their operation and perform as the efficient redundant resistance. In the operation of sleep mode, sleep transistor become OFF to cause in the reduction of leakage and dynamic power.

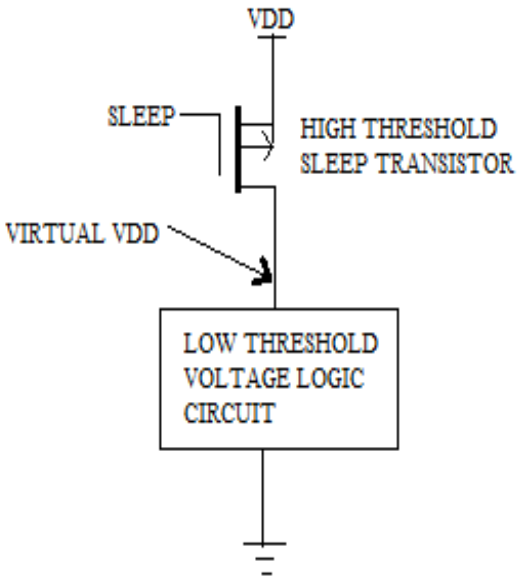

Fig 6. Header Switch

When we put the sleep transistor between supply voltage and low threshold voltage circuit module, it is known as header switch. For implementing header switch, PMOS is used as sleep transistor [12].When we put the sleep transistor between low threshold voltage circuit module and ground, it is known as Footer switch. For implementing Footer switch, NMOS is used as sleep transistor. Fig 5 and Fig 6 shows the header and footer switch.

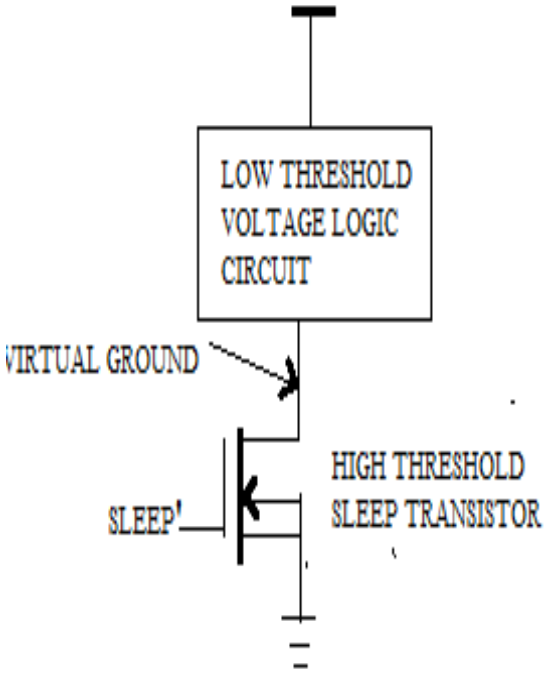

Fig 7. Footer Switch

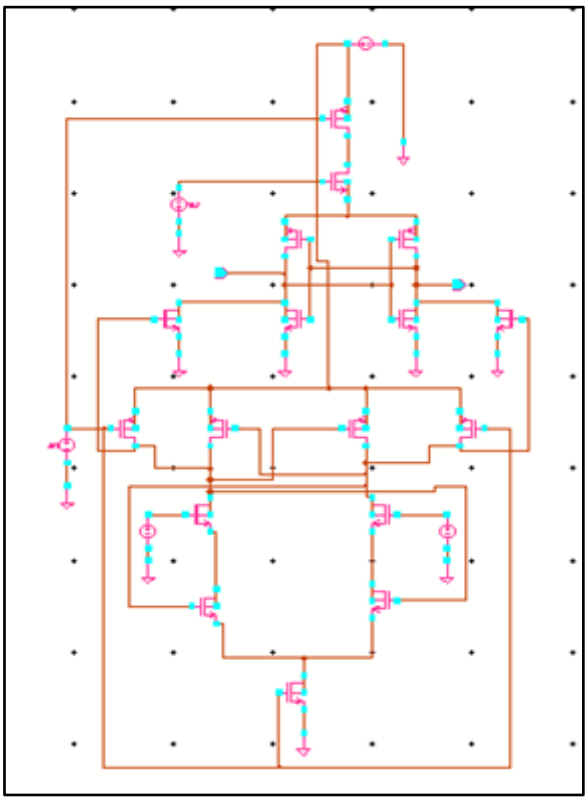

Fig 8. Schematic of Double Tail Comparator with sleep transistor

In the operation of the dual tail comparator with sleep transistors, in the time of reset phase the clock and in3 which is the input of sleep transistors is equal to zero that's why M_{tail1} and M_{tail2} are off which causes avoiding leakage power. Transistors M_1 and M_2, forces the node fn and fp to set on V_{DD}. fn and fp are the inputs of transistor

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M_{c1} and M_{c2} so transistor M_{c1} and M_{c2} will cut off. The transistors M_{R1} and M_{R2} of Intermediate stage pull down the output of both latch to ground. During decision-making phase Clock and in3 is equal to V_{DD}, so transistors $M_{tail1}$and Mt_{ail2} will become on and the sleep transistor doesn't permit V_{DD} to latch circuit.

The quantity of leakage power decreases insignificantly lesser related to suggested comparator. As we know, Power is very important part of the circuit design both analog and digital circuit face many problem to optimize the design [13-14].

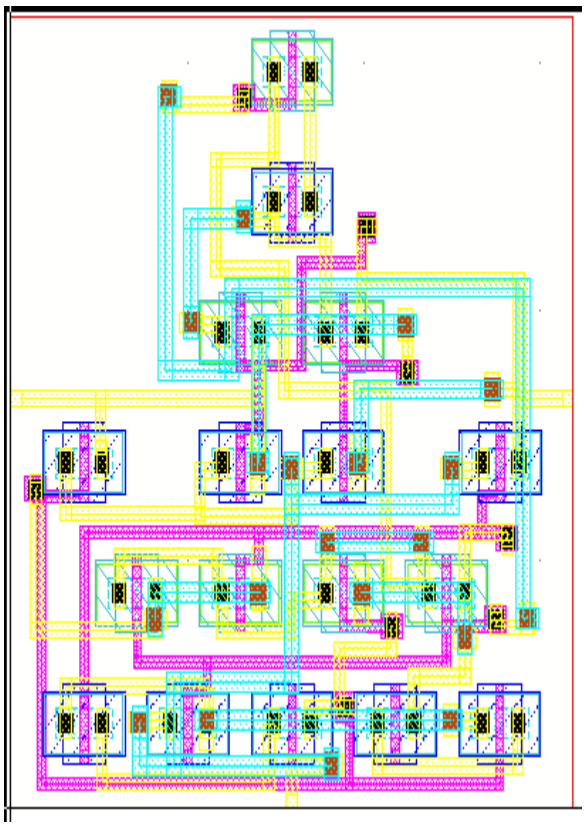

Fig.9 Layout of Double Tail Comparator with sleep transistor

IV. RESULT ANALYSIS

As the world is emerging with the several battery oriented applications, there is requirement for the handy power backup's devices so a major urge drive the research area towards reduction in power which may be accomplished by adding towards the small area consuming process[15-16]. The conventional dual tail comparator is observed by simulated in 45nm technology with supply voltage 600mV, input voltage of 300mV, reference voltage of 295mV, common mode voltage of 5mV with clock pulse of 600mV having rise time and fall time of 0.08ns and time period of 1ns.The operation of circuit is examined through the transient analysis of 3ns is shown in fig.6. It is observed from the analysis that the power consumption of this comparator design is $6.864e^{-7}$ watts and noise is $4.11569e^{-11}$.

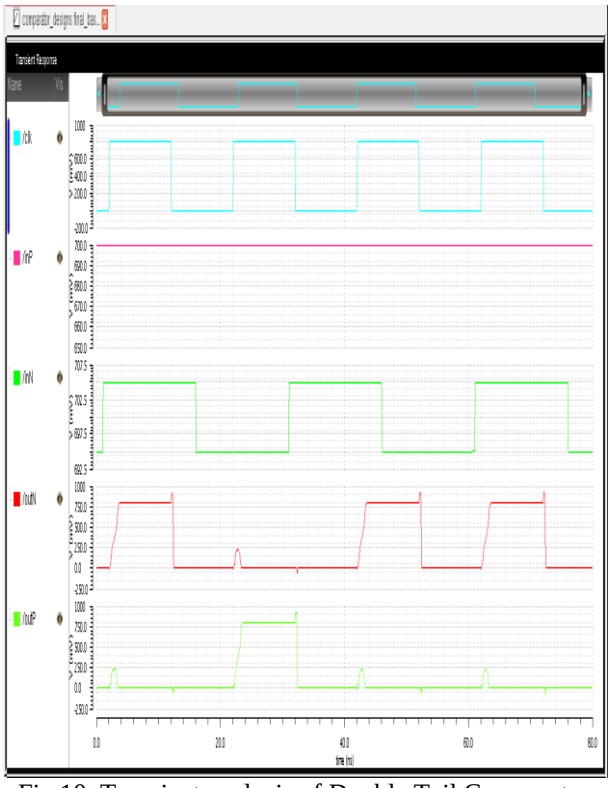

Fig 10. Transient analysis of Double Tail Comparator

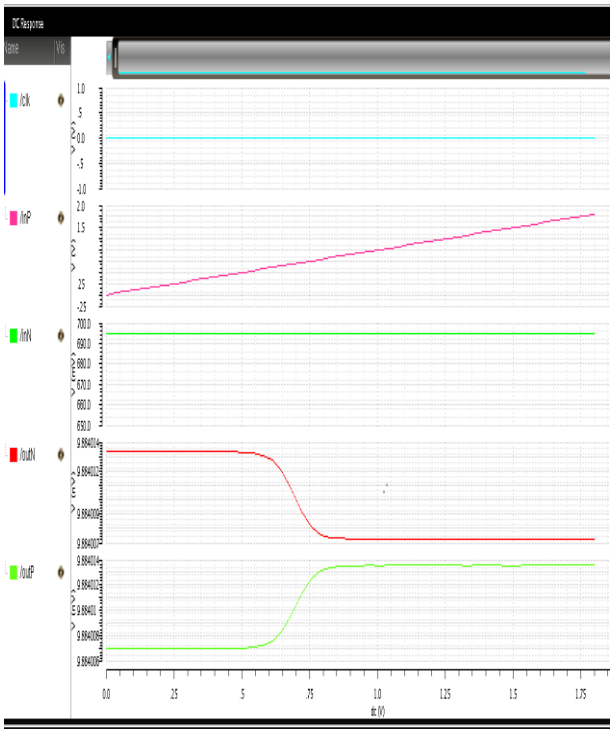

Fig 11. DC analysis of Double Tail Comparator

The dual tail comparator with sleep transistors is observed by simulated in 45nm technology with supply voltage 600mV, input voltage of 300mV, reference voltage of 295mV, common mode voltage of 5mV with clock pulse of 600mV having rise time and fall time of 0.08ns and time period of 1ns. It is observed from the analysis that the

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power consumption of this comparator design is $6.130e^{-12}$ watts and noise is $1.41017e^{-15}$.

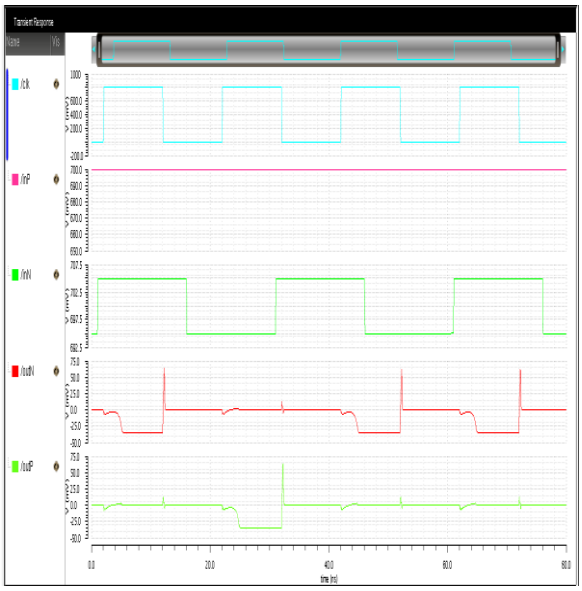

Fig 11. Simulation of Double Tail Comparator with sleep transistor

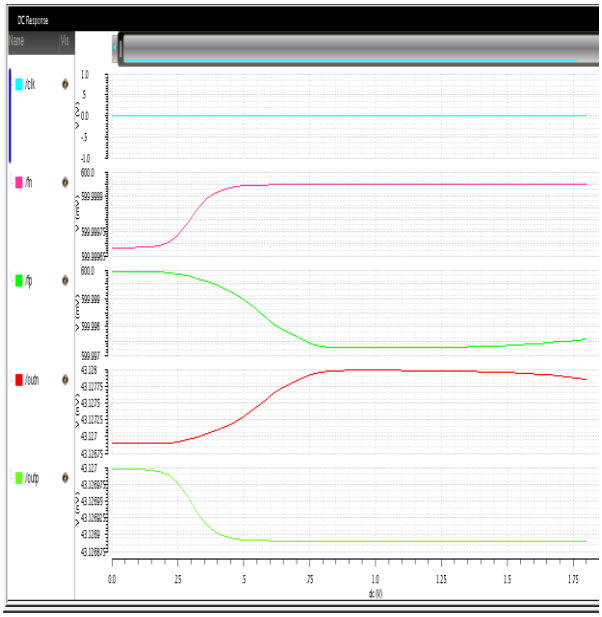

Fig 12. DC analysis of Double Tail Comparator with sleep transistor

V. CONCLUSION

From analysis of the results of the both conventional dual tail dynamic comparator which is simulated in 45nm technology with supply voltage 600mV, input voltage of 300mV, reference voltage of 295mV, common mode voltage of 5mV with clock pulse of 600mV having rise time and fall time of 0.08ns and time period of 1ns, it is observed that the power and noise is reduced in dual tail comparator with sleep transistor. It is observed that the dual tail comparator with sleep transistors give the better performance in terms of power, noise, delay, leakage power etc. In this paper we present the analysis in terms of power and noise.

Table 1. Comparative Analysis

PARAMETERS	Double Tail Comparator	Modified Designs
TECHNOLOGY	180 nm	180 nm
SUPPLY VOLTAGE	0.8 V	0.8 V
POWER	620.3 nW	169.7 nW
DELAY	346.1 ps	319.7 ps
PDP (POWER DELAY PRODUCT)	$21.468 * 10^{-17}$	$5.425 * 10^{-17}$

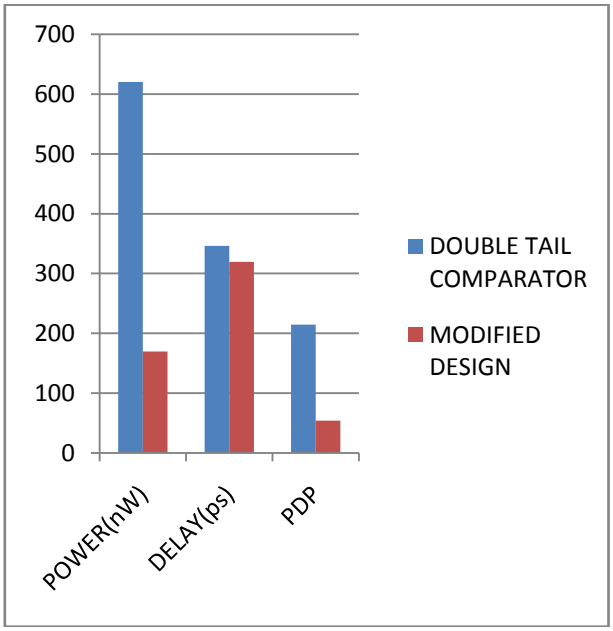

Fig 13. Comparison Chart

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BIOGRAPHIES

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